Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VCC1**
2. **A OUT**
3. **N. A OUT**
4. **A IN**
5. **A IN**
6. **N. B OUT**
7. **B OUT**
8. **VEE**
9. **B IN**
10. **B IN**
11. **B IN**
12. **C IN**
13. **C IN**
14. **N. C OUT**
15. **C OUT**
16. **VCC2**

**.045”**

**.042”**

**6 5 4 3 2**

**7**

**8**

**9**

**10**

**11 12 13**

**1**

**16**

**15**

**14**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .042” X .045” DATE: 8/8/17**

**MFG: MOTOROLA THICKNESS .025” P/N: MCC10105**

**DG 10.1.2**

#### Rev B, 7/1